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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KIM, JAY C	

ART UNIT	PAPER NUMBER
2815	

MAIL DATE	DELIVERY MODE
10/12/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	08/520,079	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	JAY C. KIM	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *87,90,123 and 126* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *87,90,123 and 126* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *28 August 1995* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Amendment filed August 10, 2011.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 87, 90, 123 and 126 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fonash et al. (US 5,275,851) in view of Sakamoto (US 5,650,664).

Regarding claim 87, Fonash et al. disclose a semiconductor device (Fig. 1) comprising a thin film transistor over a substrate (Glass substrate) comprising a crystalline semiconductor island (col. 2, lines 40-41 and 63-66, and col. 3, lines 1-6), source and drain regions in the crystalline semiconductor island (col. 3, lines 22-27), a channel forming region (center portion of Poly Si) between the source and drain regions, a gate insulating film (SiO_2) adjacent to at least the channel forming region, and a gate electrode (Gate) adjacent to the channel forming region having the gate insulating film therebetween, wherein the crystalline semiconductor island of the thin film transistor is formed in a monodomain region which contains no grain boundary, because the nickel layer 12 is formed at a bottom surface of an amorphous silicon layer to crystallize the amorphous silicon layer and can be patterned as isolated islands (col. 3, lines 1-6) and thus would not have grain boundaries shown in Fig. 2 of current

Application, wherein the crystalline semiconductor island of the thin film transistor includes nickel, because nickel in the nickel layer 12 would diffuse into the amorphous silicon layer during annealing to crystallize the amorphous silicon layer.

Fonash et al. differ from the claimed invention by not comprising a first thin film transistor provided in a matrix pixel circuit over the substrate, and a second thin film transistor provided in a peripheral driving circuit over the substrate, each of the first and second thin film transistors comprising the crystalline semiconductor island, wherein at least one of hydrogen and halogen element is contained at a concentration not higher than 1×10^{20} cm^{-3} in the monodomain regions of the first and second thin film transistors, wherein the crystalline semiconductor island of the second thin film transistor includes nickel at a concentration of 1×10^{17} cm^{-3} to 5×10^{17} cm^{-3}, wherein the crystalline semiconductor island of the first thin film transistor includes nickel at a concentration of 1×10^{16} cm^{-3} or less.

Sakamoto discloses a semiconductor device (Fig. 2) comprising a first thin film transistor provided in a matrix pixel circuit (thin film transistor formed in the pixel portion or the pixel display portion) over a substrate (71) (col. 7, lines 24-25), and a second thin film transistor provided in a peripheral driving circuit (thin film transistor formed in the peripheral logic and driver circuit) over the substrate.

Since both Fonash et al. and Sakamoto teach a semiconductor device, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the thin film transistor disclosed by Fonash et al. can be used to form an integrated circuit as disclosed by Sakamoto, because the combined semiconductor device can be

formed at a relatively low temperature requiring a relatively short annealing time and can be used in a display device. In this case, each of the first and second thin film transistors comprises the crystalline semiconductor island disclosed by Fonash et al.

Further regarding claim 87, Fonash et al. in view of Sakamoto differ from the claimed invention by not showing that at least one of hydrogen and halogen element is contained at a concentration not higher than 1×10^{20} cm^{-3} in the monodomain regions of the first and second thin film transistors, wherein the crystalline semiconductor island of the second thin film transistor includes nickel at a concentration of 1×10^{17} cm^{-3} to 5×10^{17} cm^{-3}, wherein the crystalline semiconductor island of the first thin film transistor includes nickel at a concentration of 1×10^{16} cm^{-3} or less.

It would have been obvious, if not inherent, to one of ordinary skill in the art at the time the invention was made that hydrogen is contained at a concentration not higher than 1×10^{20} cm^{-3} in the monodomain regions of the first and second thin film transistors due to contamination during deposition of the semiconductor layer and annealing, because hydrogen is a common contaminant during a semiconductor processing in an air ambient or vacuum, and can diffuse through insulating or metal layers, and also a concentration of hydrogen should be controlled to achieve a desired mobility for the thin film transistors. Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the crystalline semiconductor islands of the first and second thin film transistors may include nickel at a concentration in the claimed ranges, because a concentration of nickel can be controlled to form high quality crystalline semiconductor islands, while reducing adverse effects caused by

nickel, there is a *vertical variation* of a nickel concentration in the crystalline semiconductor islands, especially because Fonash et al. disclose that the uppermost surface 18 of the polycrystalline silicon layer is not affected by nickel (col. 2, lines 59-62), and Applicants do not *specifically* claim that nickel concentration profiles are different between the two crystalline semiconductor islands. Further regarding claim 87, the claim is *prima facie* obvious without showing that the claimed ranges of the hydrogen and nickel concentrations achieve unexpected results relative to the prior art range. *In re Woodruff*, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also *In re Huang*, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also *In re Boesch*, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and *In re Aller*, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

Regarding claim 90, Fonash et al. in view of Sakamoto further disclose that each of the crystalline semiconductor islands of the first and second thin film transistors is a silicon island.

Regarding claim 123, Fonash et al. disclose a semiconductor device (Fig. 1) comprising a thin film transistor over a substrate (Glass substrate) comprising a crystalline semiconductor island (col. 2, lines 40-41 and 63-66, and col. 3, lines 1-6), source and drain regions in the crystalline semiconductor island (col. 3, lines 22-27), a

channel forming region (center portion of Poly Si) between the source and drain regions, a gate insulating film (SiO_2) adjacent to at least the channel forming region, and a gate electrode (Gate) adjacent to the channel forming region having the gate insulating film therebetween, wherein the crystalline semiconductor island of the thin film transistor is formed in a monodomain region which contains no grain boundary, because the nickel layer 12 is formed at a bottom surface of an amorphous silicon layer to crystallize the amorphous silicon layer and can be patterned as isolated islands (col. 3, lines 1-6) and thus would not have grain boundaries shown in Fig. 2 of current Application, wherein the crystalline semiconductor island of the thin film transistor includes nickel, because nickel in the nickel layer 12 would diffuse into the amorphous silicon layer during annealing to crystallize the amorphous silicon layer.

Fonash et al. differ from the claimed invention by not comprising a first thin film transistor provided in a matrix pixel circuit over the substrate, and a second thin film transistor provided in a peripheral driving circuit over the substrate, each of the first and second thin film transistors comprising the crystalline semiconductor island, wherein each of the crystalline semiconductor islands of the first and second thin film transistors includes carbon and nitrogen at a concentration not higher than 5×10^{18} cm^{-3}, wherein each of the crystalline semiconductor islands of the first and second thin film transistors includes at least one of hydrogen and halogen element at a concentration not higher than 1×10^{20} cm^{-3} in the monodomain region, wherein the crystalline semiconductor island of the second thin film transistor includes nickel at a concentration of 1×10^{17} cm^{-}

^{3} to 5 × 10^{17} cm^{-3}, wherein the crystalline semiconductor island of the first thin film transistor includes nickel at a concentration of 1 × 10^{16} cm^{-3} or less.

Sakamoto discloses a semiconductor device (Fig. 2) comprising a first thin film transistor provided in a matrix pixel circuit (thin film transistor formed in the pixel portion or the pixel display portion) over a substrate (71) (col. 7, lines 24-25), and a second thin film transistor provided in a peripheral driving circuit (thin film transistor formed in the peripheral logic and driver circuit) over the substrate.

Since both Fonash et al. and Sakamoto teach a semiconductor device, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the thin film transistor disclosed by Fonash et al. can be used to form an integrated circuit as disclosed by Sakamoto, because the combined semiconductor device can be formed at a relatively low temperature requiring a relatively short annealing time and can be used in a display device. In this case, each of the first and second thin film transistors comprises the crystalline semiconductor island disclosed by Fonash et al.

Further regarding claim 123, Fonash et al. in view of Sakamoto differ from the claimed invention by not showing that each of the crystalline semiconductor islands of the first and second thin film transistors includes carbon and nitrogen at a concentration not higher than 5 × 10^{18} cm^{-3}, wherein each of the crystalline semiconductor islands of the first and second thin film transistors includes at least one of hydrogen and halogen element at a concentration not higher than 1 × 10^{20} cm^{-3} in the monodomain region, wherein the crystalline semiconductor island of the second thin film transistor includes nickel at a concentration of 1 × 10^{17} cm^{-3} to 5 × 10^{17} cm^{-3}, wherein the crystalline

semiconductor island of the first thin film transistor includes nickel at a concentration of 1×10^{16} cm^{-3} or less.

It would have been obvious, if not inherent, to one of ordinary skill in the art at the time the invention was made that concentrations of carbon, nitrogen and hydrogen in the crystalline semiconductor islands disclosed by Fonash et al. in view of Sakamoto may be within the claimed ranges, because carbon, nitrogen and hydrogen are common contaminants during a semiconductor processing in an air ambient or vacuum, and can diffuse through insulating or metal layers, and also concentrations of carbon, nitrogen and hydrogen should be controlled to achieve a desired mobility for the thin film transistors. Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the crystalline semiconductor islands of the first and second thin film transistors may include nickel at a concentration in the claimed ranges, because a concentration of nickel can be controlled to form high quality crystalline semiconductor islands, while reducing adverse effects caused by nickel, there is a *vertical variation* of a nickel concentration in the crystalline semiconductor islands, especially because Fonash et al. disclose that the uppermost surface 18 of the polycrystalline silicon layer is not affected by nickel (col. 2, lines 59-62), and Applicants do not *specifically* claim that nickel concentration profiles are different between the two crystalline semiconductor islands. Further regarding claim 123, the claim is *prima facie* obvious without showing that the claimed ranges of carbon, nitrogen, hydrogen and nickel concentrations achieve unexpected results relative to the prior art range. *In re Woodruff*, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also *In re Huang*, 40 USPQ2d

1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also *In re Boesch*, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and *In re Aller*, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

Regarding claim 126, Fonash et al. in view of Sakamoto further disclose that each of the crystalline semiconductor islands of the first and second thin film transistors is a silicon island.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422

F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 87, 90, 123 and 126 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-4, 6, 8, 9 and 11 of U.S. Patent No. 5,614,733 in view of Nakagawa et al. (US 4,766,477). Although the conflicting claims are not identical, they are not patentably distinct from each other because the differences between claims 87, 90, 123 and 126 of current Application and claims 1-4, 6, 8, 9 and 11 of Zhang et al. (US 5,614,733) are limitations of (i) “each of said crystalline semiconductor islands” “is formed in a monodomain region which contains no grain boundary” and (ii) recited upper limits of concentrations of hydrogen and/or halogen element, carbon and nitrogen. The concentrations of hydrogen, carbon and nitrogen in a thin film transistor are disclosed in Nakagawa et al. to form a semiconductor device having excellent semiconductor properties with high reliability and a good surface roughness (columns 3 and 4). Further, the limitations “a monodomain

region" and "grain boundary" are not well-defined and thus can be broadly interpreted to refer to active regions (comprising crystalline semiconductors) claimed in Zhang et al., and Zhang et al. would comprise "a monodomain region" and "no grain boundary" since Zhang et al. discloses substantially identical process to form "a first thin film transistor" and "a second thin film transistor".

Response to Arguments

3. Applicants' arguments filed August 10, 2011 have been fully considered but they are not persuasive.

Applicants argue that "however, the Examiner has failed to meet the burden of proof required to both establish inherency and to shift the burden to Applicants to show an unobvious difference". (1) In fact, Applicants did not specifically claim or define "monodomain" or "grain boundary" unless Applicants incorporate the claim limitations from the specification, which is improper as stipulated in MPEP 2111.01. (2) The Examiner interpreted "monodomain" as one domain, because Applicants did not specifically define what "monodomain" refers to. Applicants may have implied that a "monodomain" is one uniform single crystalline domain, but Applicants do not claim as such and Applicants' "monodomain" is not uniform in view of the original specification. Applicants' "monodomain" is obtained by diffusion of nickel as shown in Fig. 8 of current Application, and therefore there is inherently a local variation of nickel concentration, at least at an atomic scale, and crystallinity. Hence, without Applicants' further defining the limitation "monodomain", the Examiner interpreted that the "monodomain" is just one domain. (3) Also, Applicants do not specifically define what "grain boundary" is so

that one of ordinary skill in the art would be able to clearly determine whether a crystalline semiconductor island has "no grain boundary". In view of Fig. 12 of current Application, it appears that Applicants' grain boundary is a boundary where two large enough grains are in contact with each other. (4) However, as disclosed in Takemura (US 5,534,716), which was used in a Final Office Action mailed January 12, 2009 to which Applicants filed REMARKS April 13, 2009, Takemura discloses grain boundaries 6 and 7 and Applicants pointed out that Takemura teaches grain boundaries on page 8 of REMARKS filed April 13, 2009. Because Applicants disclosed the identical process for crystallization of amorphous silicon to Takemura, Applicants' "monodomain which contains no crystal grain boundary" *in fact* contains some grain boundaries similar to the grain boundaries 6 and 7 of Takemura. (5) Therefore, to avoid interpreting "a monodomain region which contains no grain boundary" too narrowly, which will lead to an enablement issue in view of Takemura, the Examiner interpreted "grain boundary" as a certain type of grain boundary which is formed when two large enough crystal grains as shown in Fig. 12 of current Application are in contact with each other. (6) In this case, when isolated nickel islands are employed for crystallization as disclosed by Fonash et al., there would not be a contact between two large enough crystal grains to form "grain boundary" as shown in Fig. 12 of current Application. (7) In sum, Applicants did not specifically define what "grain boundary" refers to, and did not specifically claim that the monodomain region does not contain a grain boundary of any type, which is not enabling in view of Takemura.

Applicants argue that “the Examiner has failed to establish that a monodomain region containing no grain boundary necessarily results from the teachings of Fonash”, that “based on these and other disclosures of Fonash, it is clear that the Examiner did not provide "cogent technical reasoning to support the conclusion of inherency", because one of ordinary skill in the art would understand that a semiconductor layer obtained by patterning a polycrystalline semiconductor would or could naturally include grain boundaries”, that “Applicants note that the term "polycrystalline" in itself even implies the existence of grain boundaries”, that “thus, the allegedly inherent characteristic of a layer having no grain boundaries would not necessarily flow from the teachings of Fonash”, that “in making this rejection, the Examiner substantially ignores the limitation of independent claims 87 and 123 relating to a monodomain region which contains no grain boundary, because "the limitations 'monodomain region' and 'grain boundary' are not defined and thus can be broadly interpreted to refer to active regions [...] claimed in Zhang et al”, that “Applicants submit, however, that one skilled in the art would dearly understand the meaning of "monodomain region" and "grain boundary", particularly in light of the specification”, and that “thus, Applicants respectfully request that the Examiner explain (1) why such terms "can be broadly interpreted to refer to active regions", and (2) why such a limitation would have been obvious over the "active region" of Zhang, in order to provide proper support this rejection”. These arguments are not convincing for the following reasons. (1) As stated above, Applicants did not specifically define what “monodomain” and “grain boundary” refer to. It is improper to import claim limitations from the specification. See MPEP 2111.01. (2) As stated

above, Applicants' "monodomain which contains no grain boundary" inherently contains grain boundaries (6 and 7) shown in Fig. 1 of Takemura, which is assigned to the same assignee with current Application as affirmed by Applicants in REMARKS filed October 16, 2009. (3) Therefore, it is clear that Applicants did not intend to exclude all the possible types of crystal grain boundaries for claims 87 and 123, and the Examiner had to interpret the "gran boundary" as a certain type of grain boundaries, not all types of grain boundaries. (4) Further, because Applicants' "monodomain" inherently comprises grain boundaries (6 and 7) of Takemura, Applicants' implied narrow definition of "monodomain" such as uniform single crystalline domain having no grain boundaries is not enabling. Therefore, the Examiner interpreted "monodomain" as just one domain. (5) Applicants' did not provide any evidence that one of ordinary skill in the art would interpret "monodomain" and "grain boundary" only in one certain way without ambiguity, and there is a universally accepted interpretation or definition of "monodomain" and "grain boundary".

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAY C. KIM whose telephone number is (571)270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. K./
Art Unit 2815
October 6, 2011

/Jerome Jackson Jr./
Primary Examiner, Art Unit 2815